BACKGROUND OF THE INVENTION

A peripheral component interconnect (PCI) bus typically has multiple peripheral devices connected thereto. The peripheral devices use the PCI bus for communications within a computer system. As the operating frequency of the PCI bus increases, bus loading on the PCI bus limits a number of peripheral devices that be connected to the PCI bus at any given time while insuring uncorrupted data communications over the PCI bus. Because of such limitations, it is difficult and costly to implement computer systems, particularly servers, that generally need many peripheral devices on the PCI bus.

Previous efforts to solve this problem include the use of bus repeaters. A bus repeater uses logic to retransmit the signals of a primary, or master, PCI bus to a secondary, or slave, PCI bus. However, bus repeaters significantly reduce useable bus bandwidth and only support a limited subset of defined PCI bus operations. The logic necessary to implement the repeater function is rather complex and thus becomes a source of system unreliability. Moreover, a bus repeater necessarily adds another PCI bus to the computer system, increasing the complexity of the computer system. Therefore, it is desirable to have a capability to handle a large number of peripheral devices on a PCI bus despite the loading problems introduced by a multi-device implementation.

SUMMARY OF THE INVENTION

From the foregoing, it may be appreciated that a need has arisen for a PCI bus implementation that is capable of having multiple peripheral devices connected thereto despite the constraints of loading limitations on the PCI bus. In accordance with the present invention, a system and method for providing access to a bus are provided that substantially eliminate or reduce disadvantages and problems associated with conventional bus implementations.

According to an embodiment of the present invention, there is provided a system for providing access to a bus that includes a bus controller with a plurality of processing devices coupled to the bus controller by a bus. A plurality of enabling switches, each associated with a corresponding processing device, are coupled to the bus. The plurality of enabling switches provide access to the bus for their corresponding processing device in response to control signals generated by the bus controller. The bus controller receives access requests from the plurality of processing devices, arbitrates the access requests according to a predetermined priority protocol, and generates a control signal corresponding to a selected access request. The control signal causes an enabling switch associated with a particular processing device that sent the selected access request to allow access to the bus for the particular processing device. The enabling switches that do not provide access to the bus make it appear that the corresponding processing devices are not coupled to the bus. Thus, processing devices not given access to the bus do not provide a load on the bus. In this manner, loading on the bus can be controlled and limited.

The present invention provides various technical advantages over conventional bus implementations. For

example, one technical advantage is to couple multiple peripheral devices to a bus that would normally cause overloading of the bus. Another technical advantage is to control a number of peripheral devices that have access to the bus. Yet another technical advantage is to use higher a frequency bus without affecting a number of peripheral devices coupled thereto. Still another technical advantage is to determine access to the bus through a priority protocol. Other technical advantages may be readily ascertainable by those skilled in the art from the following figures, description, and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings, wherein like reference numerals represent like parts, in which:

FIGURE 1 illustrates a simplified block diagram of a computer system;

FIGURE 2 illustrates a timing diagram for access to a bus of the computer system.

DETAILED DESCRIPTION OF THE INVENTION

FIGURE 1 is a block diagram of a computer system 10. Computer system 10 includes a bus controller 12, a bus 14, a plurality of processing devices 16, and a plurality of enabling switches 18. Each processing device 16 has an associated enabling switch 18 that controls when processing device 16 has access to bus 14. Each enabling switch 18 is driven by a control signal 20 generated by bus controller 12. Bus controller 12 includes arbitration logic 22 to select one of a plurality of access requests 24 received from the plurality of processing devices 16 in order to generate a control signal 20 corresponding to the selected access request 24. Enabling switches 18 may be stand alone devices, implemented within processing device 16, or implemented as part of bus 14.

In operation, processing devices 16 transmit access requests 24 to bus controller 12. Arbitration logic 22 in bus controller 12 determines which access request 24 has priority over the other access requests 24. Priority is determined according to a predetermined priority protocol that can implement a desired priority scheme using parameters that may include time of receipt if access request 24, the particular processing device 16 sending the request, and a weighting factor involving source and type of access request 24. Other parameters may be readily ascertainable by those skilled in the art and may be used as a basis in any combination to determine priority.

Arbitration logic 22 selects one of the access requests 24a received from the processing devices 16 and generates a control signal 20a associated with the selected access request 24a. Control signal 20a is provided to the enabling switch 18a corresponding to the processing device 16a that sent the selected access request 24a. Enabling switch 18a allows processing device 16a access to bus 14 in

response to control signal 20a. When processing device 16a is finished with its access to bus 14, control signal 20a disables enabling switch 18a and decouples processing device 16a from bus 14.

After arbitration logic 22 selects an access request 24a based on the priority protocol, arbitration logic 22 determines a next access request 24b according to the priority protocol. A control signal 20b is generated in response to the determination of the next access request 24b. Control signal 20b enables enabling switch 18b to provide access to bus 14 for processing device 16b. At this point in time, both processing device 16a and processing device 16b have access to bus 14. This simultaneous access to bus 14 allows processing device 16b to see when processing device 16a is through accessing bus 14. When processing device 16a completes access to bus 14, processing device 16b may now access bus 14. In this manner, idle time on bus 14 is eliminated or substantially reduced.

Arbitration logic 22 may also be used to generate control signal 20 without an associated access request 24. Such generation may be performed for various operations to include testing of computer system 10. Also, as enabling switches 18 limit access to bus 14, processing devices 16 may be removed and replaced as desired without affecting operation of bus 14. Since enabling switches 18 can make it appear that processing devices 16 are not on bus 14, installation and repair may be performed on computer system 10 during operation. Enabling switches 18 may be implemented as pass transistors or any other type of conventional switching element or apparatus.

Bus 14 is preferably a PCI bus, though any other conventional bus types may be used in computer system 10. In a conventional PCI bus implementation, the higher the

frequency of the bus operation, the smaller the number of processing devices that can be coupled to the bus at any given time. For example, four processing devices and the bus controller may be coupled to a 33 MHz PCI bus while only two processing devices and the bus controller may be coupled to a 66 MHz PCI bus. Thus, conventional PCI bus implementations provide added limitations as the desired operating frequency increases. Through the use of enabling switches 18, selection from a multitude of processing devices for coupling to bus 14 may be dynamically performed to increase a capability of computer system 10 regardless of the operating frequency of bus 14 so that higher operating frequency bus applications may be implemented.

FIGURE 2 shows a timing diagram for operation of computer system 10 with eight processing devices 16. Each processing device 16 generates an access request (PF_PCI_REQ_N(N)) upon desiring to communicate over bus 14. Arbitration logic 22 receives the access requests and selects one (PF_PCI_REQ_N(3)) based on the priority protocol. A control signal (PF_PCI_GNT_N(3)) associated with the selected access request is generated to grant access to bus 14 for the corresponding processing device 16a. Subsequently, arbitration logic 22 selects another access request (PF_PCI_REQ_N(4)) based on the priority protocol. A control signal (PF_PCI_GNT_N(4)) associated with the next selected access request is generated to provide access to bus 14 for its corresponding processing device 16b. Processing devices 16a and 16b have simultaneous access to bus 14 at this time. Processing device 16a completes its data transfer over bus 14 while processing device 16b awaits its turn to access bus 14. Upon completion of data transfer, access to bus 14 for processing device 16a is disabled and processing device 16b begins its data transfer over bus 14. This operating

scenario is repeated for all access requests received by bus controller 12.

Thus, it is apparent that there has been provided, in accordance with the present invention, a system and method for providing access to a bus that satisfies the advantages set forth above. Although the present invention has been described in detail, it should be understood that various changes, substitutions, and alterations may be readily ascertainable by those skilled in the art and may be made herein without departing from the spirit and scope of the present invention as defined by the following claims.